# SystemVerilog for Verification: A Guide to Learning the Testbench Language Features

*Chris Spear, Greg Tumbush*

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Based on the highly successful second edition, this extended edition of *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill.

In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include:

• New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard
• Descriptions of UVM features such as factories, the test registry, and the configuration database
• Expanded code samples and explanations
• Numerous samples that have been tested on the major SystemVerilog simulators

*SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition* is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.

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