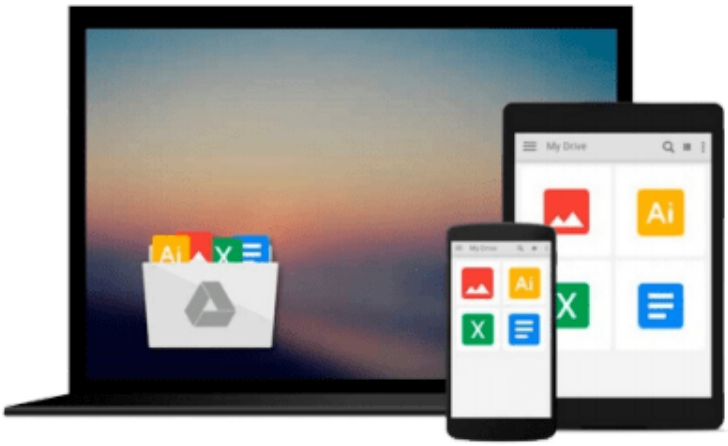

SystemVerilog for Design and Verification using UVM: From RTL to Synthesis

Mark A. Azadpour

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SystemVerilog for Design and Verification using UVM: From RTL to Synthesis Mark A. Azadpour This book is an “A-Z” guide to using SystemVerilog for ASIC design, from conception to RTL coding, to synthesis and verification. Readers will benefit from a thorough introduction to the powerful constructs and features of SystemVerilog. In addition, the verification methodology of Universal Verification Methodology (UVM) is used to build test-benches that allow for verification of complicated designs and synthesis basics are discussed, using the Synopsys Design Compiler (DC). To complete this book’s package as a practical guide, readers are introduced to the fundamentals of static timing analysis.

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